WHAT IS CLAIMED IS:

1. A semiconductor package comprising:

a plurality of horizontal metal leads, each lead having a first side, an opposite second side, and an inner end, wherein the inner ends of the leads each face a central region in a horizontal plane of the leads;

a first semiconductor chip having input/output pads, said first chip located in the central region;

a second semiconductor chip having central input/output pads and peripheral input/output pads, wherein each of the central input/output pads superimposes and is electrically connected to a respective one of the input/output pads of the first semiconductor chip, and each of the peripheral input/output pads superimposes and is electrically connected to the first side of a respective one of the leads; and

a package body formed of a hardened encapsulating material, wherein the first and second semiconductor chips are encapsulated in the package body, and at least a portion of the second side of each of the leads is exposed at a horizontal first exterior surface of the package body.

2. The semiconductor package of claim 1, wherein the second side of each lead includes at least one recessed horizontal surface covered by said encapsulating material.

3. The semiconductor package of claim 1, wherein the second side of each lead includes a recessed horizontal surface at the inner end of the lead, said recessed horizontal surface being covered by said encapsulating material.

4. The semiconductor package of claim 1, wherein the second sides of the leads exposed at said first exterior surface collectively form rows and columns.

5. The semiconductor package of claim 1, wherein the second side of each lead includes at least one recessed horizontal surface covered by said encapsulating material and at least two surfaces exposed at the first exterior surface of the package.

6. The semiconductor package of claim 1, wherein a surface of the first semiconductor chip is exposed at the first exterior surface of the package body, and a surface of the second semiconductor chip is exposed at an opposite second exterior surface of the package body.

7. The semiconductor package of claim 1, wherein a surface of at least one of the first and second semiconductor chips is exposed at an exterior surface of the package body.

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8. The semiconductor package of claim 1, wherein the input/output pads of the first chip are each electrically connected to the central input/output pads of the second chip, and the peripheral input/output pads of the second chip are each electrically connected to the first side of the lead, by a reflowed metal ball or an anisotropic conductive film.

9. The semiconductor package of claim 1, wherein a first surface of the first semiconductor chip is exposed at the first exterior surface of the package body, said first surface being covered by a layer of a conductive paste, and each exposed portion of the second side of each lead has a conductive ball thereon.

10. The semiconductor package of claim 1, wherein each exposed portion of the second side of each lead has a conductive ball thereon.

11. The semiconductor package of claim 1, further comprising an insulative layer on the first side of each lead, wherein the peripheral input/output pads of the second semiconductor chip are electrically connected to the first side of the lead through said insulative layer.

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12. A semiconductor package comprising:

a chip mounting plate having a first side and an opposite second side;

a plurality of horizontal metal leads, each lead having a first side, an opposite second side, and an inner end facing the chip mounting plate;

a first semiconductor chip having a first surface and an opposite second surface, wherein the first surface includes central input/output pads and peripheral input/output pads and the second surface is mounted on the first side of the chip mounting plate;

a second semiconductor chip having a first surface with input/output pads thereon, wherein each of the input/output pads of the second semiconductor chip superimposes and is electrically connected to a respective one of the central input/output pads of the first semiconductor chip;

a plurality of metal wires each electrically connected between the first side of a respective one of the leads and a respective one of the peripheral bond pads of the first semiconductor chip; and

a package body formed of a hardened encapsulating material, wherein the first and second semiconductor chips are encapsulated in the package body, and at least a portion of the second side of each of the leads is exposed at a horizontal first exterior surface of the package body.

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13. The semiconductor package of claim 12, wherein the second surface of the first semiconductor chip superimposes the first side of the leads.

14. The semiconductor package of claim 12, wherein the second side of each lead includes at least one recessed horizontal surface covered by said encapsulating material.

15. The semiconductor package of claim 12, wherein the second side of each lead includes a recessed horizontal surface at the inner end of the lead, said recessed horizontal surface being covered by said encapsulating material.

16. The semiconductor package of claim 12, wherein the second sides of the leads exposed at said first exterior surface collectively form rows and columns.

17. The semiconductor package of claim 12, wherein the second side of each lead includes at least one recessed horizontal surface covered by said encapsulating material and at least two surfaces exposed at the first exterior surface of the package.

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18. The semiconductor package of claim 12, wherein a central portion of the second side of the chip mounting plate is exposed at the first exterior surface of the package body, and a surface of the second semiconductor chip is exposed at an opposite second exterior surface of the package body.

19. The semiconductor package of claim 12, wherein a surface of the second semiconductor chip is exposed at a second exterior surface of the package body.

20. The semiconductor package of claim 12, wherein the second surface of the first semiconductor chip is supported on the first side of the leads by an insulative layer, said insulative layer being covered by said encapsulating material.

21. The semiconductor package of claim 12, wherein the central input/output pads of the first chip are each electrically connected to the input/output pads of the second chip by a reflowed metal ball or an anisotropic conductive film.

22. The semiconductor package of claim 12, wherein a portion of the second side of the chip mounting plate is exposed at the first exterior surface of the package body,

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said portion being covered by a layer of a conductive paste, and the exposed portion of the second side of each lead has a conductive ball thereon.

23. The semiconductor package of claim 12, wherein each exposed portion of the second side of each lead has a conductive ball thereon.

24. The semiconductor package of claim 12, wherein the second side the chip mounting plate includes a central surface and a recessed horizontal surface surrounding the central surface, and said recessed horizontal surface is covered by said encapsulating material.

25. The semiconductor package of claim 12, wherein the second side the chip mounting plate includes a central surface exposed at the first exterior surface of the package body, and a recessed horizontal surface surrounding the central surface, and said recessed horizontal surface is covered by said encapsulating material.

26. The semiconductor package of claim 25, wherein the second surface of the first semiconductor chip superimposes the first side of the leads.

27. The semiconductor package of claim 25, wherein the second side of each lead includes at least one recessed horizontal surface covered by said encapsulating material.

28. A semiconductor package comprising:

a plurality of horizontal metal leads, each lead having a first side, an opposite second side, and an inner end wherein the second side of each lead includes at least one recessed horizontal surface and the inner ends of the leads face a central chip placement region;

first and second semiconductor chips stacked in said chip placement region, each said chip having input/output pads, wherein at least some of the input/output pads of the first semiconductor chip face and are electrically connected to respective ones of the input/output pads of the second semiconductor chip by a first conductor, and other input/output pads of one of the first and second semiconductor chips are over the first side of the leads and are electrically connected to the first side of a respective ones of leads by a second conductor; and

a package body formed of a hardened encapsulating material, wherein the first and second semiconductor chips and the conductors are encapsulated in the package body, the recessed horizontal surface of each of the leads is covered by the encapsulating material, and at least a

portion of the second side of each of the leads is exposed at a horizontal first exterior surface of the package body.

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29. The semiconductor package of claim 28, further comprising a chip mounting plate in said chip placement region and having a first side and an opposite second side, wherein the first and second semiconductor chips are stacked on the first side of the mounting plate, and the second side the chip mounting plate includes a central surface exposed at the first exterior surface of the package body and a recessed horizontal surface surrounding the central surface, said recessed horizontal surface being covered by said encapsulating material.

30. The semiconductor package of claim 28, wherein the input/output pads over the first side of the leads each face and are electrically connected to the first side of the lead.

31. The semiconductor package of claim 28, wherein the first conductor is a reflowed metal ball or an anisotropic conductive film, and the second conductor is a metal wire.

32. The semiconductor package of claim 28, wherein the first and second conductors are an anisotropic conductive film.

33. The semiconductor package of claim 28, wherein one of the first and second semiconductor chips is in a horizontal plane with the leads in said chip placement region.